Unit 8

Combinational Circuit Design and

Simulation Using Gates

Outline

- Review of combinational circuit design
- Design of circuits with limited gate fan-in
- Gate delay and timing diagrams
- Hazards in combinational logic
- Simulation and testing of logic circuits

Review of Combinational Circuit Design

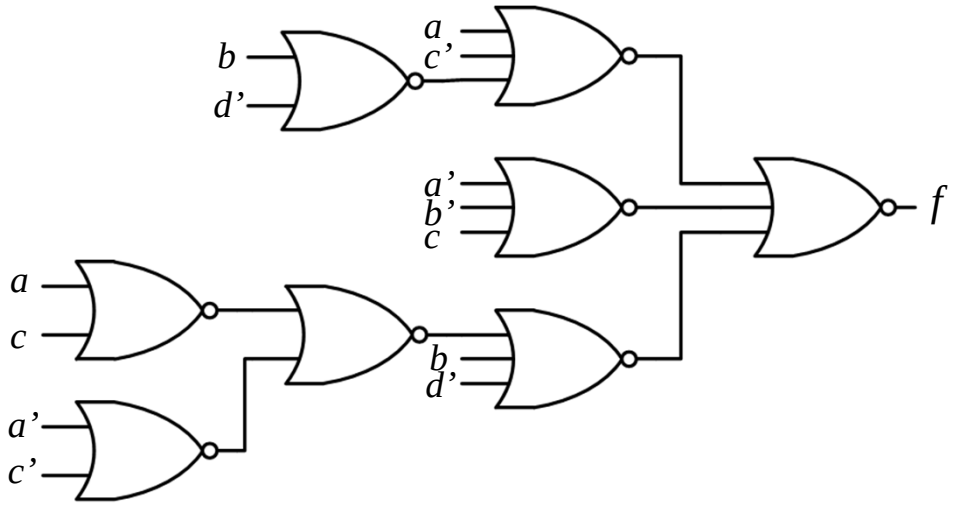
- Design of a combinational switching circuit
  - Setup a truth table which specifies the output(s) as a function of the input variables
  - Derive simplified algebraic expressions for the output functions using K-Maps, the Q-M method, or other similar procedures.
- Multi-level & Multi-output circuit
- Minimum SOP's starting point
  - Minimum two-level AND-OR、NAND-NAND、OR-NAND、NOR-OR
- Minimum POS's starting point
  - Minimum two-level OR-AND、NOR-NOR、AND-NOR、NAND-AND

Circuit with Limited Gate Fan-In (1/3)

- Ex 1

  Realize $f(a,\ b,\ c,\ d)=\sum m(0,\ 3,\ 4,\ 5,\ 8,\ 9,\ 10,\ 14,\ 15)$ using 3-input NOR gates

ab \ cd	00	01	11	10
00	1	1	0	1
01	0	1	0	1
11	1	0	1	0
10	0	0	1	1

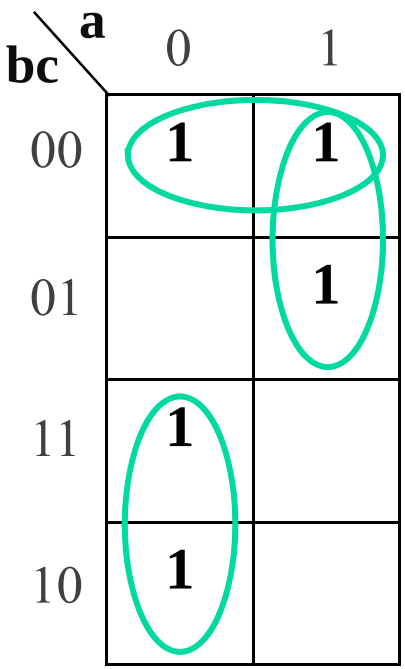


$$f' = a'b'c'd + ab'cd + abc' + a'bc + a'cd'$$

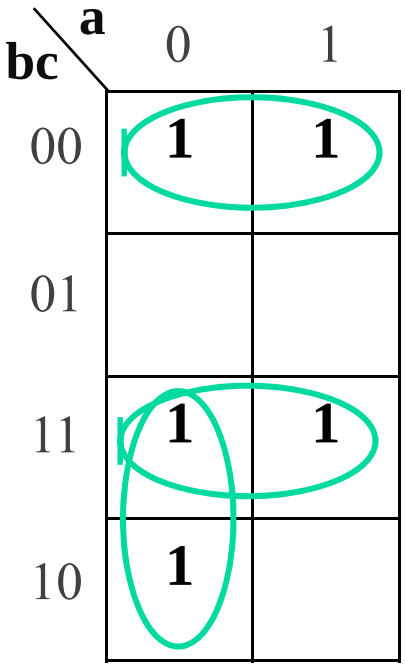
$$= b'd(a'c' + ac) + a'c(b + d') + abc'$$

Circuit with Limited Gate Fan-In (2/3)

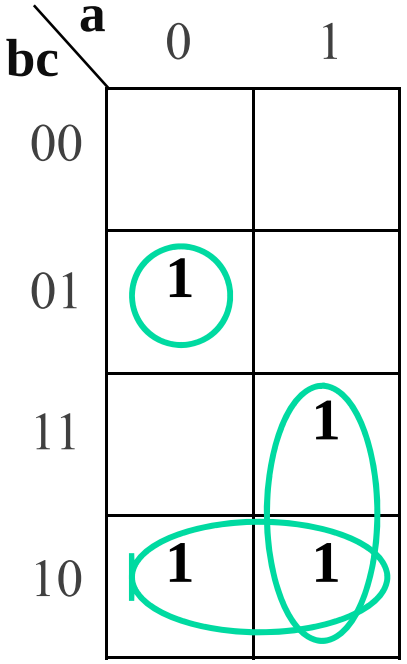
- Ex 2
  Only using 2-input NAND gates and inverters



$f_1 = \sum m(0, 2, 3, 4, 5)$



$f_2 = \sum m(0, 2, 3, 4, 7)$



$f_3 = \sum m(1, 2, 6, 7)$

$f_1 = b'c' + ab' + a'b$

$f_2 = b'c' + bc + a'b$

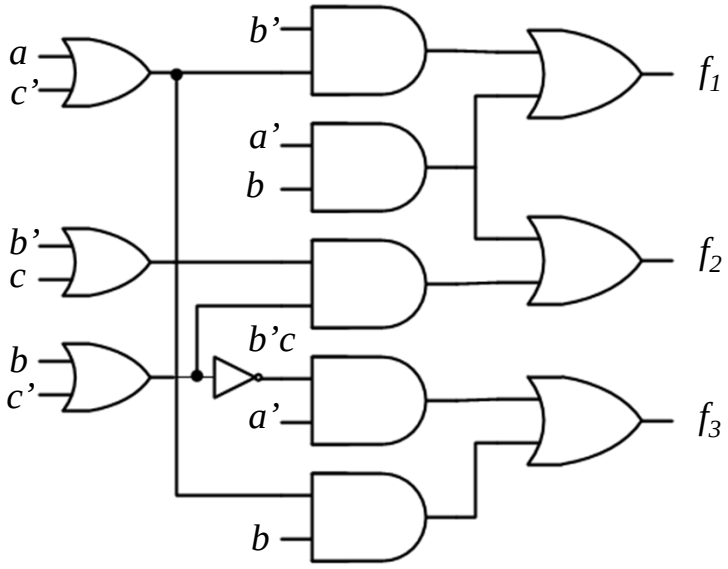
$f_3 = a'b'c + ab + bc'$

Circuit with Limited Gate Fan-In (3/3)

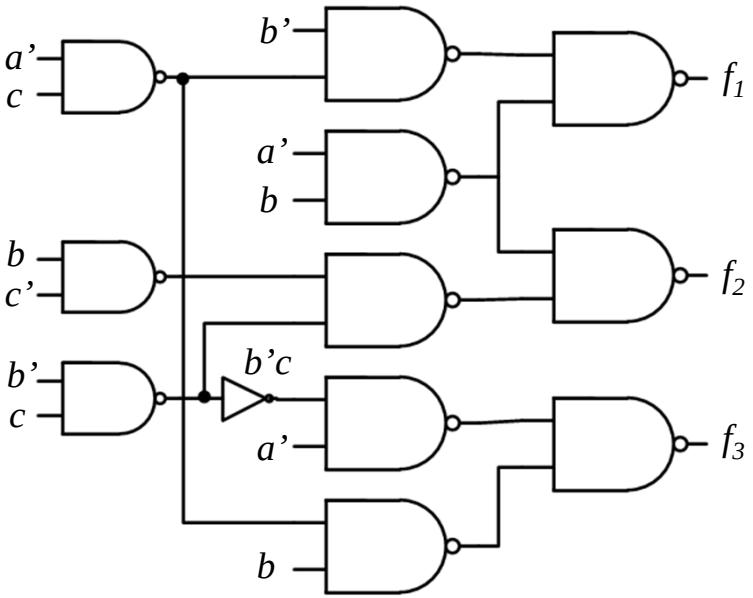
$$f_1 = b'(a + c') + a'b$$

$$f_2 = b(a' + c) + b'c' \quad \text{or} \quad f_2 = (b' + c)(b + c') + a'b$$

$$f_3 = a'b'c + b(a + c')$$

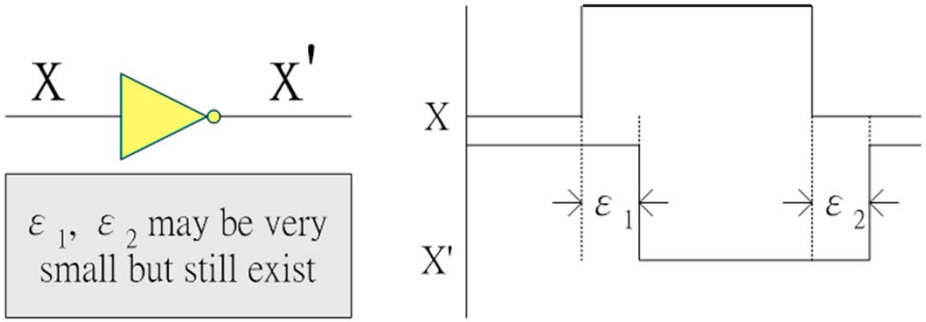


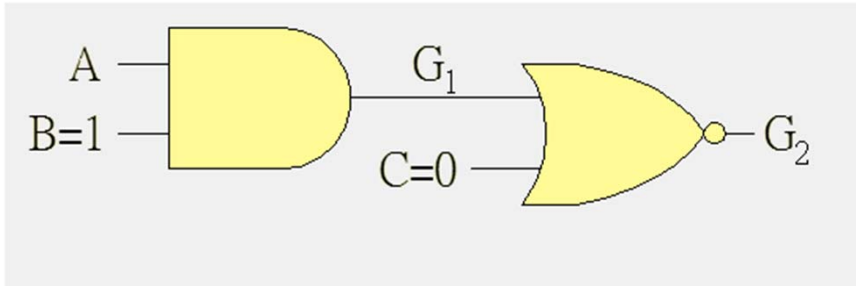
(a)

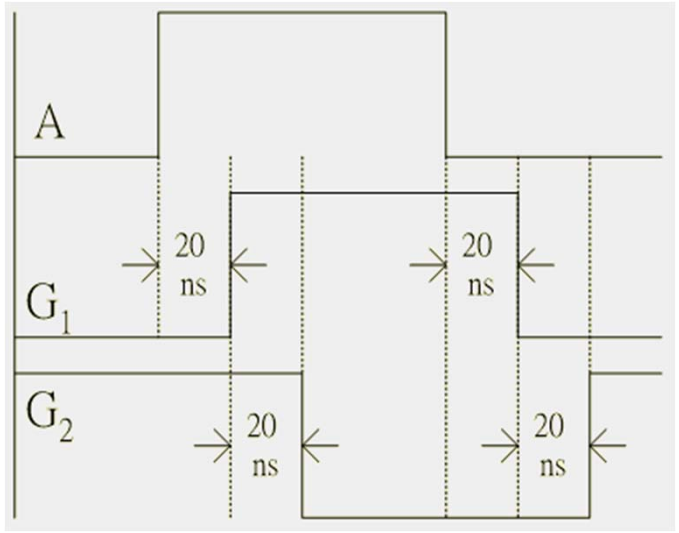


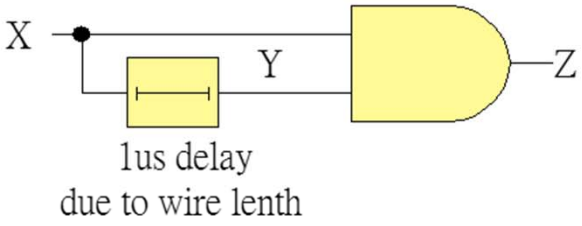
(b)

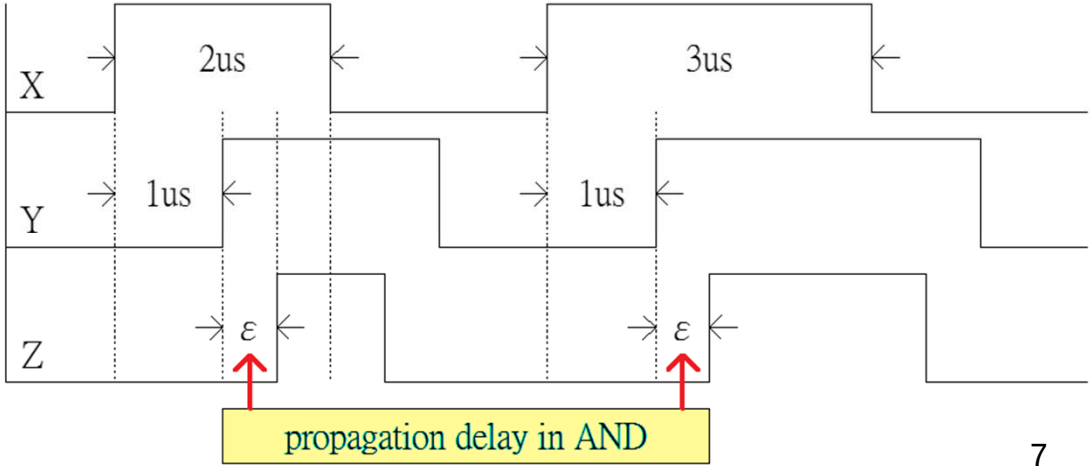
Gate Delay and Timing Diagrams (1/2)





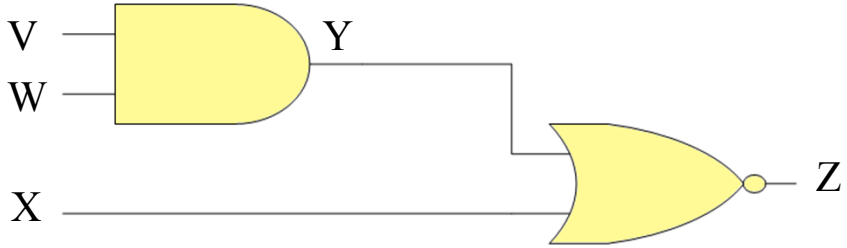


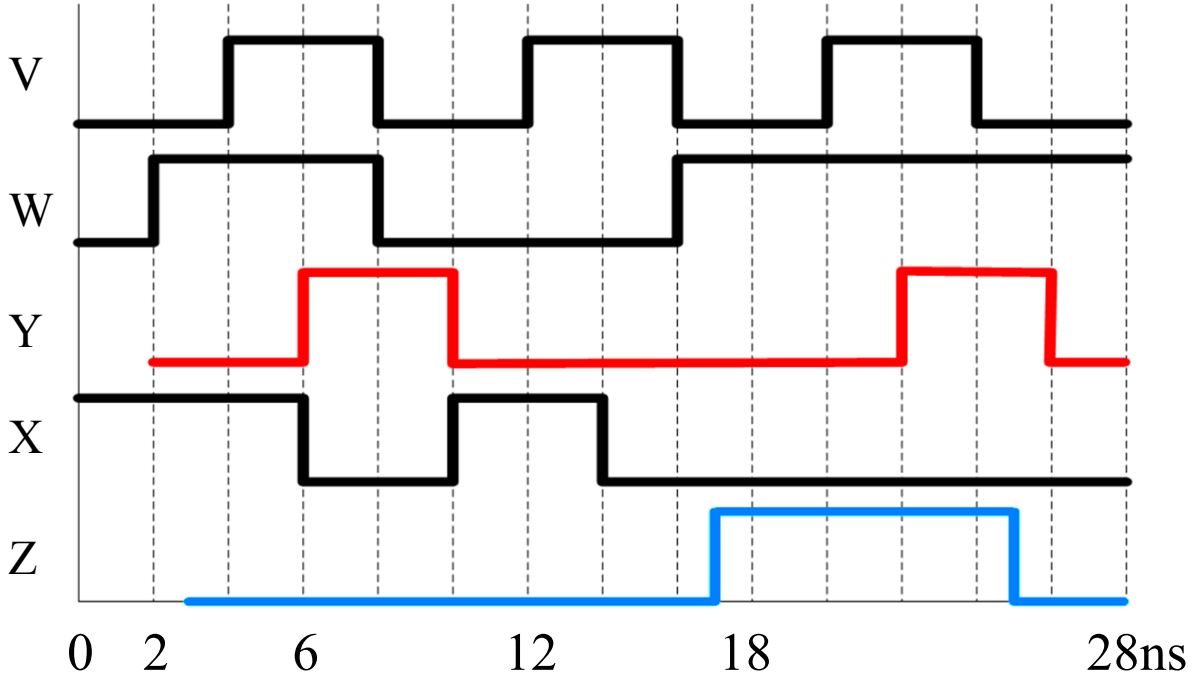




Gate Delay and Timing Diagrams (2/2)

AND = 2ns
NOR = 3ns

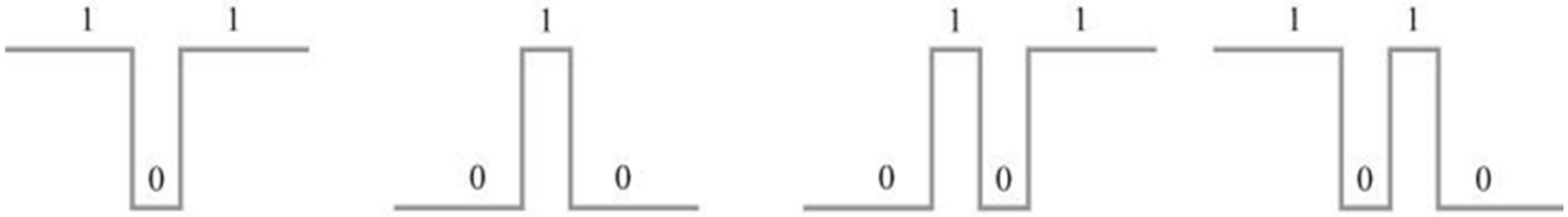




If x signal is complemented, what happen to z ?

Hazard in Combinational Logic (1/5)

- What is hazard?
  - **Unwanted** switching transients appearing in the output while the input to a combinational circuit changes
- Types of hazards

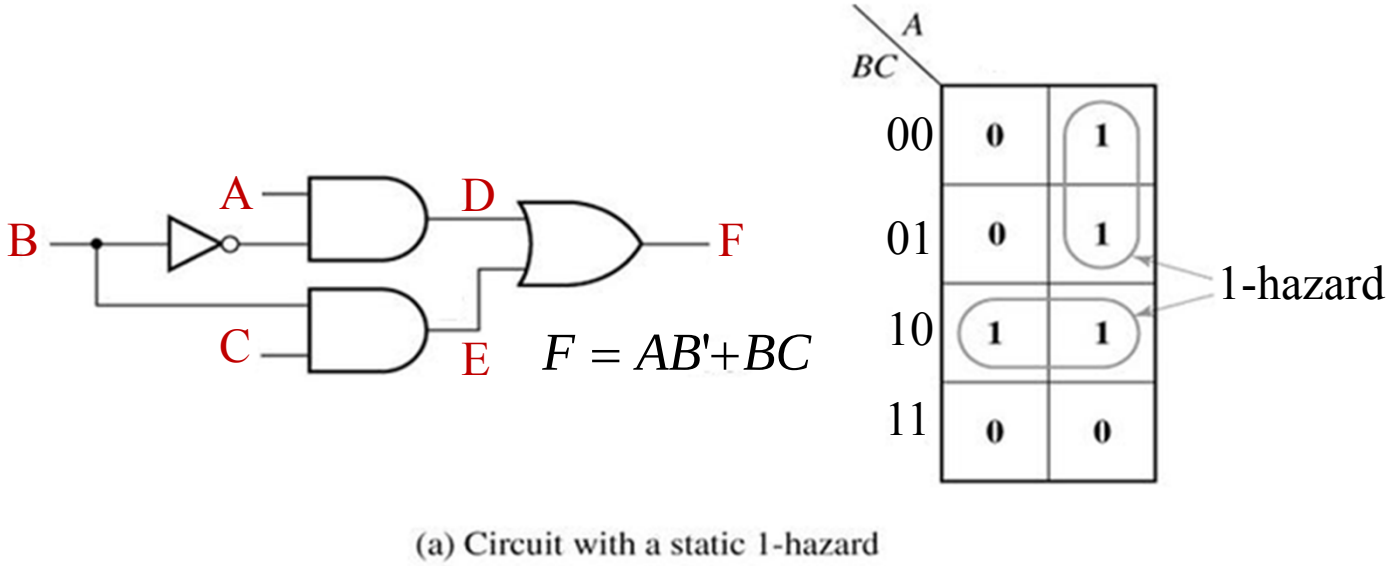


(a) Static 1-hazard (b) Static 0-hazard (c) Dynamic hazards

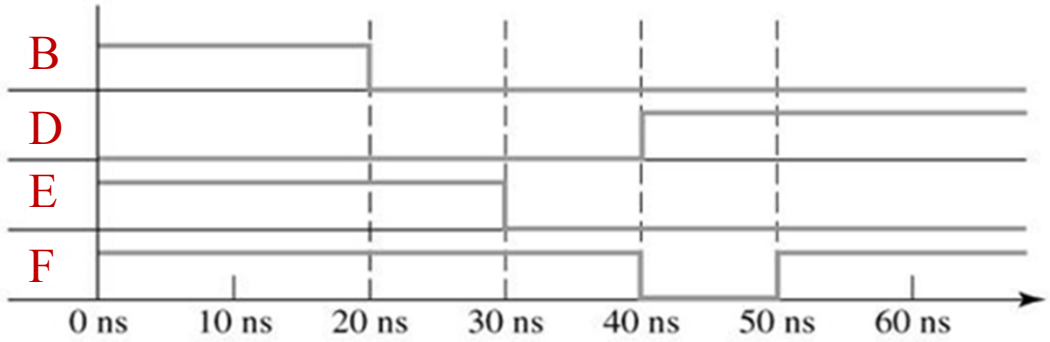
- In K-Map,
  - If any two adjacent 1's are not covered by the same loop, a 1-hazard exists for the transition between the two 1's.

Hazard in Combinational Logic (2/5)

- Let A=1 and C=1 (Static 1-hazard)



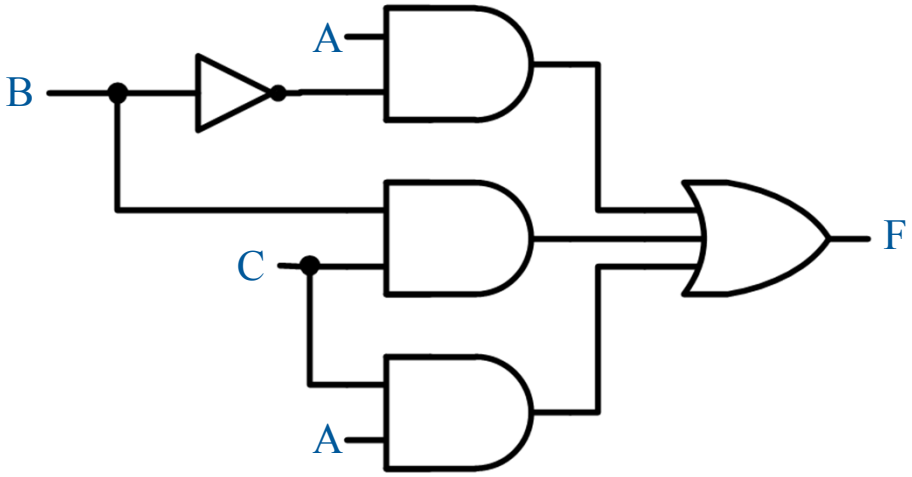
(a) Circuit with a static 1-hazard



(b) Timing chart

Hazard in Combinational Logic (3/5)

Circuit with hazard removed

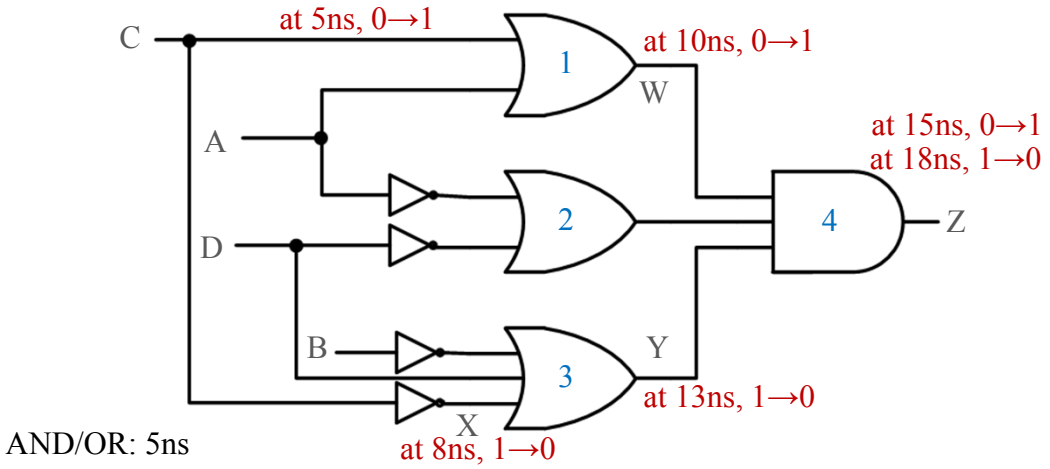


BC \ A	0	1
00	0	1
01	0	1
11	1	1
10	0	0

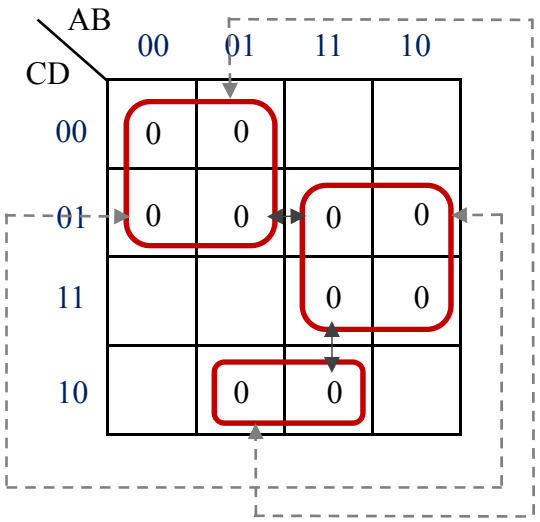
$$F = AB' + BC + AC$$

Hazard in Combinational Logic (4/5)

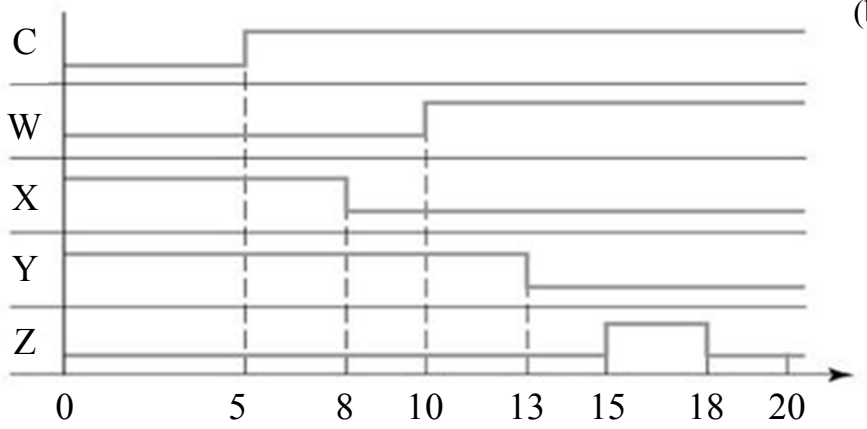
- Let A=0, B=1, and D=0 (Static 0-hazard)



(a) Circuit with a static 0-hazard



(b) Karnaugh map for circuit of (a)

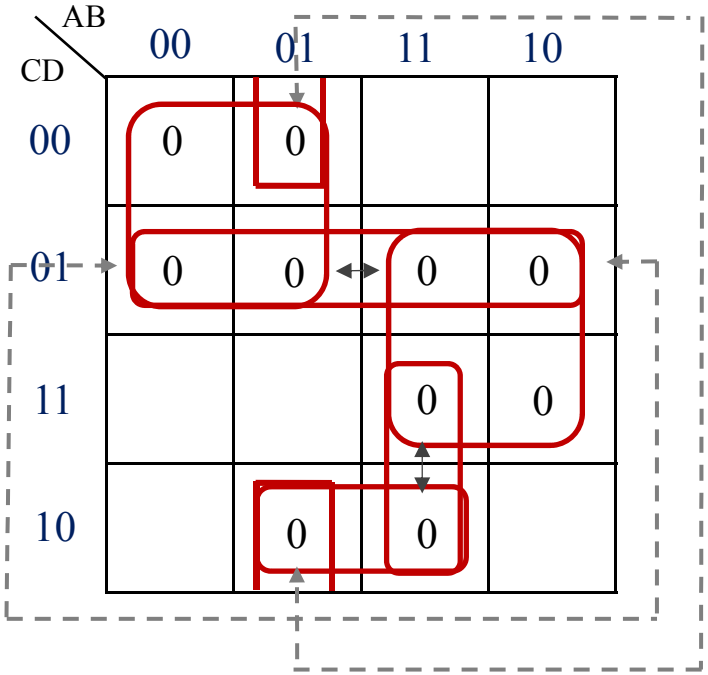


(c) Timing diagram illustrating 0-hazard of (a)

Hazard in Combinational Logic (5/5)

Circuit with hazard removed

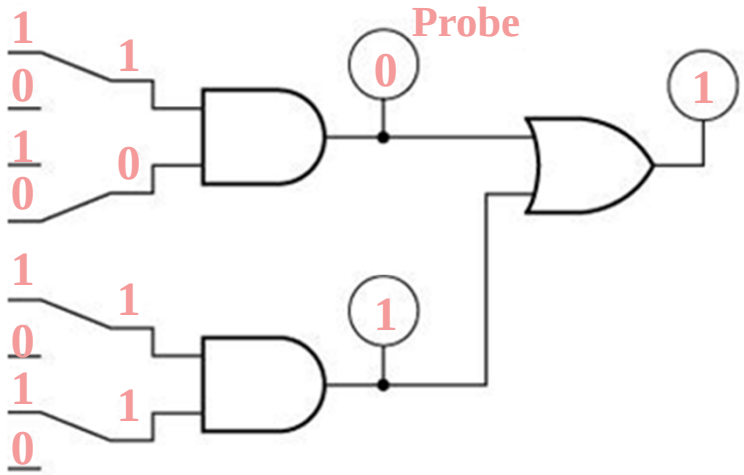
$$F = (A+C)(A'+D')(B'+C'+D)$$



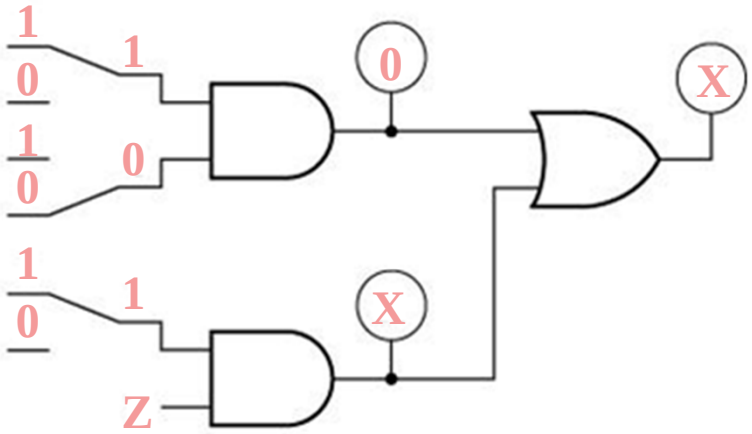
$$F = (A+C)(A'+D')(B'+C'+D)(C+D')(A+B'+D)(A'+B'+C')$$

Simulation and Testing of Logic Circuits (1/4)

- For simulating logic circuits
  - Specify the circuit components and connections
  - Determine the circuit inputs
  - Observe the circuit outputs
- 4-valued logic simulator
  - 0 (low)、1 (high)、X (unknown)、Z (high impedance)



(a) Simulation screen showing switches



(b) Simulation screen with missing gate input

AND & OR function for 4-valued simulation

•	0	1	X	Z
0	0	0	0	0
1	0	1	X	X
X	0	X	X	X
Z	0	X	X	X

+	0	1	X	Z
0	0	1	X	X
1	1	1	1	1
X	X	1	X	X
Z	X	1	X	X

Simulation and Testing of Logic Circuits (3/4)

- In the logic circuit, a wrong output may be due to
  - Verification
    - Incorrect design
    - Gates connected wrong
    - Wrong input signals to the circuit
  - Testing
    - Defective gates
    - Defective connecting wires

Simulation and Testing of Logic Circuits (4/4)

- Logic circuit with incorrect output
  - A = B = C = D = 1, F=0